



## VLSI BACKEND 2016 Projects List

S.NO	IEEE TITLE	YEAR
STSVB01	New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements	2016
STSVB02	Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell	2016
STSVB03	Graph-Based Transistor Network Generation Method for Supergate Design	2016
STSVB04	Design of Full Adder circuit using Double Gate MOSFET	2016
STSVB05	Dual Use of Power Lines for Design-for-Testability—A CMOS Receiver Design	2016
STSVB06	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	2016
STSVB07	A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy	2016
STSVB08	A Low-Voltage Radiation-Hardened 13T SRAM Bit cell for Ultralow Power Space Applications	2016
STSVB09	Fast and Wide Range Voltage Conversion in Multi supply Voltage Designs	2016
STSVB10	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	2016
STSVB11	Low-Power and Area-Efficient Shift Register Using Pulsed Latches	2016
STSVB12	Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology	2016
STSVB13	Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit	2016
STSVB14	Single-Supply 3T Gain-Cell for Low-Voltage Low-Power Applications	2016